REMARKS

Claims 1-23 were pending in this application. Claims 17 and 22 were canceled. New Claims 24-30 were added. Claims 1-16, 18-21, 23-30 will remain after this amendment.

Figure 4 was objected to because element "400" was not mentioned in the description. The specification has been amended to specify "pipeline 400" in reference to Figure 4.

The title "EFFICIENT EMULATION DISPATCH BASED ON INSTRUCTION WIDTH" was objected to as being not descriptive. The title has been amended to "EFFICIENT EMULATION INSTRUCTION DISPATCH BASED ON INSTRUCTION WIDTH" to overcome the objection.

Claims 7, 9, 16 and 21 were objected to under 35 USC 112 for reciting "RTI." These Claims have been amended to specify "run-test idle."

The pending Claims have been amended to clarify certain aspects. The amendments are supported by the specification. No new matter has been added. Claim 1 has been amended to clarify that the instructions are "emulation instructions." "Emulation instructions" are shown in Fig. 5 and described on pages 8-14 of the specification.

Claims 1-7, 9-14, 16-19 and 21-23 were rejected under 35 USC 103(a) as being unpatentable over Shang in view of Iizuka.

In general, Shang does not teach "emulation instructions" or an "emulation instruction register," as recited in Claim 1. The Office Action acknowledges that Shang does not teach "receiving a plurality of instructions simultaneously from the emulation instruction register;" "providing the first instruction of the plurality of instructions to the processor if the first instruction is valid;" or "providing the second

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instruction of the plurality of instructions to the processor if the second instruction is valid," as recited in Claim 1.

The Office Action cites Iizuka as teaching "receiving a plurality of instructions simultaneously from the emulation instruction register." But Iizuka does <u>not</u> teach "<u>emulation</u> instructions" or an "<u>emulation</u> instruction register," as recited in Claim 1. Claim 1 further recites "determining <u>a</u> validity of a first <u>emulation</u> instruction of the plurality of <u>emulation</u> instructions by reading <u>width bits in the first emulation instruction</u>," which is not disclosed by Shang or Iizuka. Thus, Applicants respectfully submit that amended Claim 1 is allowable over Shang and Iizuka.

Claims 2-8 depend from Claim 1 and are allowable for the reasons stated above.

In addition, Shang and Iizuka do not teach "storing the plurality of emulation instructions in the emulation instruction register <u>in subsequent clock cycles</u>," as recited in amended Claim 3.

Shang and Iizuka do not teach "<u>loading</u> the plurality of emulation instructions <u>in parallel</u> into the emulation instruction register," as recited in Claim 5.

Shang and Iizuka do not teach "providing the plurality of <u>emulation</u> instructions to the decoder <u>after a first run-test idle state</u> without <u>entering into a second run-test idle state</u>, as recited in amended Claim 7. Shang and Iizuka do not teach a "run-test idle" state.

Independent Claim 9 is not taught by Shang and Iizuka because neither reference teaches the "run-test idle state signal" in Claim 9.

Shang and Iizuka do not teach "an N-bit emulation instruction register," as recited in Claim 10.

Claims 11-15 depend from Claim 9 and are believed to be allowable for the reasons stated above.

Independent Claim 16 is not taught by Shang and Iizuka because neither reference teaches the "emulation instructions," "emulation control logic," and "detection of a single run-test idle state" in amended Claim 16.

Claims 18-20 depend from Claim 16 and are believed to be allowable for the reasons stated above.

Independent Claim 21 is not taught by Shang and Iizuka because neither reference teaches the "emulation instructions" and "emulation instruction register" of Claim 21.

Claims 23-24 depend from Claim 21 and are believed to be allowable for the reasons stated above.

New Claims 24-30 have been added and are supported by the specification. No new matter has been added. Claims 24-30 depend from independent Claims 1, 16 and 21 and are believed to be allowable for the reasons stated above.

Applicants respectfully request that all pending Claims be allowed. Enclosed is a $90.00 check for additional claim fees.

Please apply any additional charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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ALEX CHEN
REG NO 45,591

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